

ABSTRACT

A stack package of the present invention is made by stacking at least two area array type chip scale packages. Each chip scale package of an adjacent pair of chip scale packages is attached to the other in a manner that the ball land pads of the upper stacked chip scale package face in the opposite direction to those of the lower stacked chip scale package, and the circuit patterns of the upper stacked chip scale package are electrically connected to the those of the lower stacked chip scale package by, for example, connecting boards. Therefore, it is possible to stack not only fan-out type chip scale packages, but to also efficiently stack ordinary area array type chip scale packages.